ABSTRACT

A display apparatus and a method for driving the display apparatus that are capable of suppressing image quality degradation resulting from delay in sampling pulses or from waveform rounding thereof and image quality degradation caused by coupling between the signal line and the common line and that between the signal line and the scan line even when the simultaneous sampling number is increased. The start pulse HST has a pulse width that includes a plurality of pulse widths of the clock pulses HCK and HCKX, for example, two pulse widths. The clock pulses DCK have four phases. Large margins $\alpha 1$ and $\alpha 2$ in the phase relationship between each of the clock pulses DCK1 to DCK4 and each of transfer pulses used for extracting the clock pulses DCK1 to DCK4 are assured. As a result, even if delay or waveform rounding occurs in the clock pulses DCK1 to DCK4, sampling pulses SP1 to SP6 with a constant pulse width equal to that of each of the clock pulses DCK1 to DCK4 can be generated without being affected by the delay or waveform rounding.